ABSTRACT

Disclosed is a programmable logic circuit control apparatus capable of managing data with various bit widths and data lengths, generated by various processes to be executed by a programmable logic circuit, with a simple structure. A module address memory section (4) stores data indicating addresses of modules or conditions for branching processes and jump distances page by page. A write address and a read address of an internal data memory (2) are also stored in a page where the address of a module is stored. A circuit control section (5) reads data of each page from the module address memory section (4), and, according to the read data, reads a module, reconfigures a programmable logic circuit and reads data of a next page, or performs jump. When the programmable logic circuit is to be reconfigured, the circuit control section (5) performs an operation of supplying a write address and a read address to the internal data memory (2).